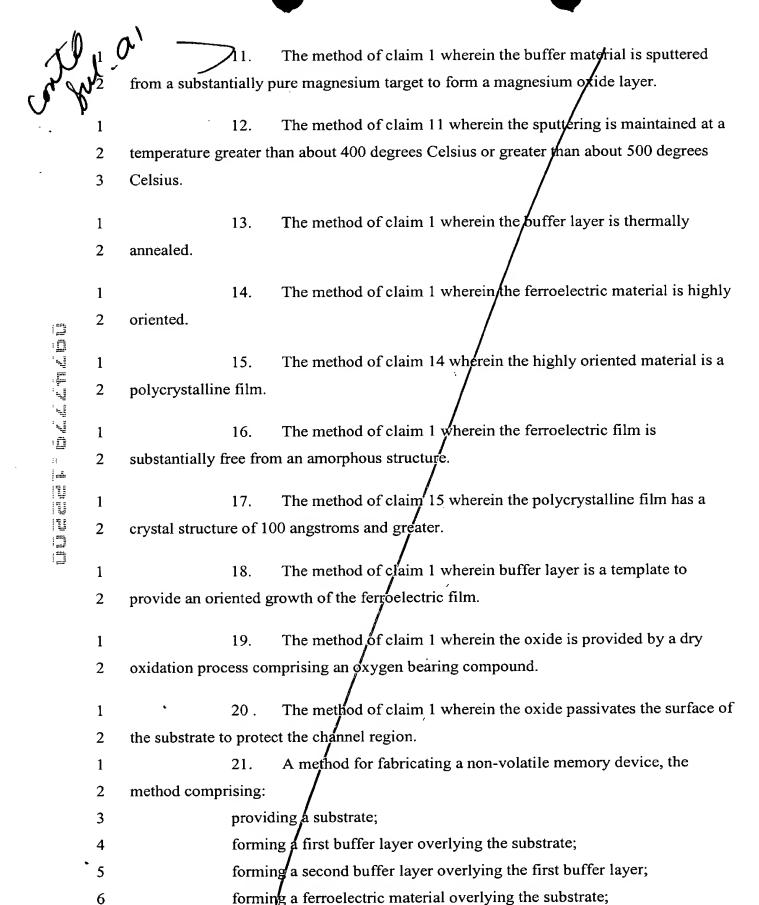
WHAT IS CLAIMED IS:

T	1. A method for fabricating a non-volatile memory device, the
2	method comprising:
3	providing a substrate;
4	forming an oxide layer overlying the substrate;
5	forming a buffer layer overlying the oxide layer;
6	forming a ferroelectric material overlying the substrate;
7	forming a gate layer overlying the ferroelectric material, the gate layer
8	overlying a channel region; and
9	forming a first source/drain region adjacent to a first side of the channel
10	region and a second source/drain region adjacent to a second side of the channel region.
1	2. The method of claim 1 wherein the channel region is about 1
2	micron and less.
1	3. The method of claim 1 wherein the ferroelectric material is a PZT
2	bearing compound.
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1	4. The method of claim 1 wherein the buffer layer is a magnesium
2	bearing compound.
1	5. The method of claim 1 wherein the buffer layer is a magnesium
2	oxide layer, the magnesium oxide layer being a barrier layer.
1	6. The method of claim 1 wherein the ferroelectric material has a
2	thickness of less than about 1,000 Angstroms.
1	7. The method of claim 1 wherein the buffer layer has a thickness
2	ranging from about 7 to 100 nanometers.
1	8. The method of claim 1 wherein the ferroelectric material has a
2	thickness of about 100 Angstroms and greater.
1	9. The method of claim 1 wherein the ferroelectric material is PZT.
1	10. The method of claim 1 wherein the buffer layer is a barrier
2	diffusion layer, the barrier diffusion layer substantially preventing diffusion between the
3	ferroelectric material to the substrate.



forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and 8 forming first and second doped regions adjacent to first and second ends of 9 the channel region. 10 22. The method of claim 21, wherein the first buffer layer is a gate 1 oxide layer, and the second buffer layer is a MgO layer. 2 23. The method of claim 21, wherein the first buffer layer is an 1 amorphous layer, and the second buffer layer is a highly-oriented layer. 2 The method of claim 23, wherein the second buffer layer has a 1 24. 2 thickness of no more than 10 hm. A memory structure for integrated circuit devices, the structure 25. 1 2 comprising: 3 a substrate; an oxide layer overlying the substrate; 4 a buffer layer overlying the oxide layer; 5 a ferroelectric material overlying the substrate; 6 = a gate layer overlying the ferroelectric material, the gate layer overlying a 7 channel region; and 8 a first source/drain region adjacent to a first side of the channel region and 9 a second source/drain region adjacent to a second side of the channel region. 10

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